AMENDMENTS TO THE CLAIMS

Please reconsider the double patent rejection of the claims as shown below. A complete listing of all pending claims is presented.

1. (Original) A semiconductor memory apparatus comprising:

a memory unit having unit blocks each including:

a memory core including a plurality of memory cells laid out to form a cell matrix; and

redundant lines including redundant memory cells each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein:

said unit blocks are further laid out to form a block matrix or a plurality of block matrixes, and every plurality of said unit blocks forms a one-dimensional group oriented in a first direction (row or column direction) or a second direction (column or row direction); and

said redundant lines are shared by said unit blocks pertaining to said one-dimensional group;

self-test means mounted in the same chip as said memory unit to serve as embedded self-test means for evaluating said memory cells in order to determine whether said memory cells are good or defective; and

self-repair means mounted in said same chip as said memory unit to serve as embedded self-repair means for:

selecting only a minimum number of address pairs among address pairs received from said embedded self-test means as address pairs each including a first-direction address (row or column address) and second-direction address (column or row address) of an abnormal memory cell;

storing said selected minimum number of address pairs in first storage means for each of said unit blocks as address pairs required for determining a redundant line to be used for repairing an abnormal memory cell; and

finding a redundant line to be used for repairing an abnormal memory cell for each of said unit blocks on the basis of address pairs stored in said first storage means.

2. (Original) A semiconductor memory apparatus according to claim 1, wherein:

said embedded self-repair means has a first storage unit and a first shift-register unit;

said first storage unit is capable of storing a maximum number of possible different second-direction addresses selected from address pairs stored in said first storage means for all said unit blocks pertaining to said one-dimensional group on the assumption that said unit blocks form said one-dimensional group oriented in said second direction and said redundant lines connected in said second direction are shared by said unit blocks pertaining to said one-dimensional group;

said first shift-register unit has as many shift registers as said redundant lines connected in said second direction;

each of said shift registers has as many shift stage bits as said maximum number; and

said first shift-register unit sequentially points to one of said second-direction addresses stored in said first storage unit by shifting said shift registers; and

said first shift-register unit generates a pattern of an address set of said second-direction address by operating only one of said shift registers at a time.

3. (Original) A semiconductor memory apparatus according to claim 2, wherein:

an address set generated as an address set of a second-direction address is reported for all said unit blocks and, if an address pair including said second-direction address exists in said first storage means, said address pair is assumed to be an address pair that can be repaired by using a redundant line connected in said second direction; and

if an address pair remains in said first storage means as an unrepairable address pair to be repaired, said address pair remaining to be repaired is examined to determine whether or not said unrepairable address pair remaining to be repaired can be repaired by using a redundant line connected in said first direction.

4. (Original) A semiconductor memory apparatus according to claim 3, wherein:

as means to determine whether or not it is possible to use a redundant line connected in said first direction for repairing a remaining address pair, which cannot be repaired by using a redundant line connected in said second direction, said embedded self-repair means is provided with as many second storage units as said redundant lines connected in said first direction for each of said unit blocks as second storage units each used for storing a first-direction address; and

said embedded self-repair means executes the steps of:

supplying a first-direction address of a remaining address pair which cannot be repaired by using a redundant line connected in said second direction to said second storage units;

discarding said first-direction address of said remaining address pair if said first-direction address has already been stored in said second storage units;

determining that said remaining address pair can be repaired by using a redundant line connected in said first direction if said first-direction address thereof can be accommodated in said second storage units; and

determining that said remaining address pair cannot be repaired by using a redundant line connected in said first direction if said first-direction address thereof cannot be accommodated in said second storage units.

5. (Original) A semiconductor memory apparatus according to claim 3, wherein:

as means to determine whether or not it is possible to use a redundant line connected in said first direction for repairing a remaining address pair, which cannot be repaired by using a redundant line connected in said second direction, said embedded self-repair means is provided with as many first-direction shift registers independent of each other as said redundant lines connected in said first direction for each of said unit blocks; and

said embedded self-repair means executes the steps of:

shifting any of said first-direction shift registers and taking a first-direction address pointed to by said first-direction shift registers as a first-direction repair address;

determining whether or not a remaining address pair, which cannot be repaired by using a redundant line connected in said second direction, can be repaired by using a redundant line connected in said first direction as a redundant line corresponding to said first-direction repair address; and

further shifting any of said first-direction shift registers and determining whether or not said remaining address pair can be repaired if said remaining address pair cannot be repaired by using said redundant line connected in said first direction.

6. (Original) A semiconductor memory apparatus according to claim 2, wherein said shift registers of said first shift-register unit each have not only as many shift stage bits as said possible different second-direction addresses but also an additional shift stage bit for indicating a state in which no redundant lines connected in said second direction are used.

7. (Previously presented) A semiconductor memory apparatus according to claim 2, wherein:

a plurality of said shift registers employed in said first shift-register unit are named a first shift register, a second shift register, a third register and so on;

with said first shift register fixed, after said second shift register, said third shift register and so on are shifted, said first shift register is shifted by 1 bit and, after said first shift register is shifted by 1 bit, an operation to shift said second shift register is started from a shift-stage position coinciding with a new shift-stage position of said first shift register or a shift-stage position immediately following said new shift-stage position of said first shift register, and an operation to shift said third shift register is started from a shift-stage position coinciding with said start shift-stage position of said second shift register or a shift-stage position immediately following said start shift-stage position of said second shift register.

8. (Original) A semiconductor memory apparatus according to claim 1, wherein:

on the assumption that said unit blocks form a one-dimensional group in said second direction, as many shift-register flags as said redundant lines connected in said second direction

are provided for each of address pairs storable in said first storage means provided for all said unit blocks pertaining to said one-dimensional group;

said shift-register flags are linked to each other to form as many shift registers each having a chain form spread over all said unit blocks as said redundant lines connected in said second direction;

said shift registers form a second shift-register unit; and

an address set of said second-direction address is generated by shifting said shift registers of said second shift-register unit one register after another.

9. (Original) A semiconductor memory apparatus according to claim 8, wherein said shift registers of said second shift-register unit each have not only as many shift stage bits as said address pairs storable for all said unit blocks pertaining to said one-dimensional group, but also an additional shift stage bit for indicating a state in which no redundant lines connected in said second direction are used.

10. (Original) A semiconductor memory apparatus according to claim 8, wherein:

a plurality of said shift registers employed in said second shift-register unit is named a first shift register, a second shift register, a third register and so on;

said embedded self-repair means executes;

with said first shift register fixed, after said second shift registers, said third shift registers and so on are shifted, said first shift register is shifted by 1 bit and, after said first shift register is shifted by 1 bit, an operation to shift said second shift register is started from a shift-stage position coinciding with a new shift-stage position of said first shift register or a shift-stage position immediately following said new shift-stage position of said first shift register, and an operation to shift said third shift register is started from a shift-stage position coinciding with said start shift-stage position of said second shift register or a shift-stage position immediately following said start shift-stage position of said second shift register.

11. (Original) A semiconductor memory apparatus according to claim 8, wherein:

said embedded self-repair means has a duplication flag provided for each of address pairs storable in said first storage means provided for all said unit blocks;

said duplication flags are each used to indicate that an address pair associated with said duplication flag includes a second-direction address stored at 2 or more storage locations in said first storage means;

when any particular one of said shift registers employed in said second shift-register unit is shifted to a next shift stage position coinciding with one of said duplication flags, which have been put in a set state, said next shift stage position is ignored and said particular shift register is shifted again.

12. (Original) A semiconductor memory apparatus according to claim 11, wherein:

said embedded self-repair means reports a second-direction address pointed to by said shift registers employed in said second shift-register unit for all of said unit blocks; and

if said reported second-direction address exists also in said first storage means for another one of said unit blocks, said duplication flag of said other unit block is set.

13. (Original) A semiconductor memory apparatus according to claim 8, wherein:

said embedded self-repair means reports a second-direction address pointed to by said second shift-register unit for all of said unit blocks while shifting said second shift-register unit;

if the same second-direction address as said reported second-direction address already exists in said first storage means, said embedded self-repair means assumes that an address pair including said same second-direction address is a repairable address pair;

said embedded self-repair means determines whether or not a remaining address pair, if any, can be repaired; and

if a remaining address pair cannot be repaired, said embedded self-repair means again shifts said second shift-register unit and again determine whether or not said remaining address pair can be repaired.

14. (Original) A semiconductor memory apparatus according to claim 8, wherein said embedded self-repair means has a special flag provided for each of address pairs storable in said first storage means for all of said unit blocks as a flag to be set to indicate that a second-direction address of an address pair associated with said special flag matches an address set of a second-direction address reported by said embedded self-repair means for all of said unit blocks and is thus regarded as a second-direction repair address.

15. (Original) A self-repair method adopted in a semiconductor memory apparatus comprising:

a memory unit having unit blocks each including:

a memory core including a plurality of memory cells laid out to form a cell matrix; and

redundant lines including redundant memory cells each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein:

said unit blocks are further laid out to form a block matrix or a plurality of block matrixes, and every plurality of said unit blocks forms a one-dimensional group oriented in a first direction (row or column direction) or a second direction (column or row direction); and

said redundant lines are shared by said unit blocks pertaining to said one-dimensional group; and

self-test means mounted in the same chip as said memory unit to serve as embedded self-test means for evaluating said memory cells in order to determine whether said memory cells are good or defective,

said self-repair method comprising:

a first process of selecting address pairs among address pairs received from said embedded self-test means as address pairs each including a first-direction address (row or column address) and second-direction address (column or row address) of an abnormal memory cell and storing said selected address pairs in first storage means for each of said unit blocks as address pairs required for determining a redundant line to be used for repairing an abnormal memory cell;

a second process of generating a pattern of an address set of a second-direction address on the basis of said second-direction address of an address pair stored in said first storage means on the assumption that said unit blocks form said one-dimensional group oriented in said second direction;

a third process of reporting an address set generated in said second process as an address set of a second-direction address for all said unit blocks and determining whether or not an address pair of an abnormal memory cell unrepairable by said address set can be repaired by using any of said redundant lines connected in said first direction for all said unit blocks; and

a fourth process of generating a next address set to be used next in said process third process if a determination result of said third process indicates that an unrepairable address pair is found in any of said unit blocks;

whereby said first to fourth processes are sequentially carried out repeatedly to determine whether or not all address pairs of abnormality memory cells for all said unit blocks can be repaired.

16. (Original) A self-repair method according to claim 15, whereby said first process is carried out to select only a minimum number of address pairs among address pairs received from said embedded self-test means as address pairs required for determining a redundant line to be used for repairing an abnormal memory cell and store said selected minimum number of address pairs in said first storage means for each of said unit blocks.

17. (Original) A self-repair method adopted in a semiconductor memory apparatus comprising:

a memory unit having unit blocks each including:

a memory core including a plurality of memory cells laid out to form a cell matrix; and

redundant lines including redundant memory cells each used for repairing an abnormal memory cell generated in any of said memory cores,

wherein:

said unit blocks are further laid out to form a block matrix or a plurality of block matrixes, and every plurality of said unit blocks forms a two-dimensional group oriented in a first direction (row or column direction) or a second direction (column or row direction); and

said redundant lines are shared by said unit blocks pertaining to said two-dimensional group; and

self-test means mounted in the same chip as said memory unit to serve as embedded self-test means for evaluating said memory cells in order to determine whether said memory cells are good or defective,

said self-repair method comprising:

a first process of selecting address pairs among address pairs received from said embedded self-test means for said unit blocks, a plurality of which or every plurality of which forms a two-dimensional group, as address pairs each comprising a first-direction address (row or column address) and second-direction address (column or row address) of an abnormal memory cell, and storing said selected address pairs in first storage means for each of said unit blocks as address pairs required for determining a redundant line to be used for repairing an abnormal memory cell by executing the steps of:

condensing said second-direction address so that said unit blocks arranged in said first direction appear as one apparent unit block;

arranging a plurality of said apparent unit blocks into a one-dimensional array oriented in said second direction; and

storing address pairs of abnormal memory bits for said apparent unit blocks arranged in said one-dimensional array oriented in said second direction in said first storage means;

a second process of generating a pattern of an address set of a second-direction address on the basis of said second-direction address of an address pair stored in said first storage means;

a third process of reporting an address set generated in said second process as an address set of a second-direction address for all said unit blocks and determining whether or not an address pair of an abnormal memory cell left unrepaired by using said address set can be repaired by using any of said abundant lines connected in said first direction for all said unit blocks; and

a fourth process of generating a next address set to be used next in said process third process if a determination result of said third process indicates that an address pair left unrepaired is found in any of said unit blocks;

whereby said first to fourth processes are sequentially carried out repeatedly to determine whether or not all address pairs of abnormality memory cells for all said unit blocks can be repaired.

18. (Original) A self-repair method according to claim 17, whereby said first process is carried out to select only a minimum number of address pairs among first-direction and second-direction address pairs received from said embedded self-test means as address pairs required for determining a redundant line to be used for repairing an abnormal memory cell, convert said selected minimum number of address pairs and store said converted minimum number of address pairs in said first storage means for each of said apparent unit blocks.